IXYS

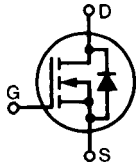
HiPerFET™ Power MOSFETs
ISOPLUS247™
(Electrically Isolated Back Surface)

IXFR 30N50Q
IXFR 32N50Q

V_{DSS}	I_{D25}	$R_{DS(on)}$
500 V	29 A	0.16 Ω
500 V	30 A	0.15 Ω

$t_{rr} \leq$ 250 ns

N-Channel Enhancement Mode
High dV/dt, Low t_{rr}, HDMOS™ Family

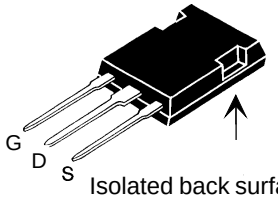


Preliminary data

Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		500	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C	30N50 32N50	30	A
I_{DM}	T_C = 25°C, Pulse width limited by T_{JM}	30N50 32N50	120	A
I_{AR}	T_C = 25°C	30N50 32N50	30	A
E_{AS}	T_C = 25°C		1.5	J
E_{AR}	T_C = 25°C		45	mJ
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \leq V_{DSS}$ $T_J \leq$ 150°C, R_G = 2 Ω		5	V/ns
P_D	T_C = 25°C		310	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s		300	°C
V_{ISOL}	50/60 Hz, RMS t = 1 minute leads-to-tab		2500	V~
Weight			6	g

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 1mA		500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4mA		2		4	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$ V_{GS} = 0 V	T_J = 25°C T_J = 125°C			100 1	µA mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = I_T$ Notes 1, 2	30N50 32N50			0.16 0.15	Ω Ω

ISOPLUS 247™
E 153432



Isolated back surface*

G = Gate D = Drain
S = Source

* Patent pending

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Low drain to tab capacitance(<50pF)
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Fast intrinsic Rectifier

Applications

DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control

Advantages

- Easy assembly
- Space savings
- High power density

IXYS reserves the right to change limits, test conditions, and dimensions. 98608B (7/00)

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Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; $I_D = I_T$	Note 2	18	28		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz			3950		pF
C_{oss}				640		pF
C_{rss}				210		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, $I_D = I_T$			35		ns
t_r	R_G = 1 Ω (External),			42		ns
$t_{d(off)}$				75		ns
t_f				20		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, $I_D = I_T$			150		nC
Q_{gs}				26		nC
Q_{gd}				85		nC
R_{thJC}					0.40	K/W
R_{thCK}				0.15		K/W

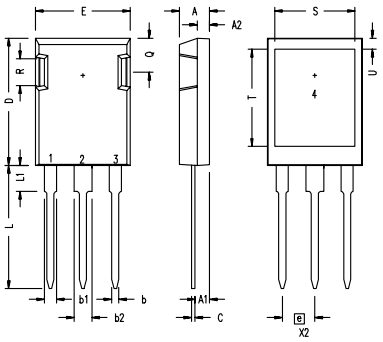
Source-Drain Diode — Characteristic Values (T_J = 25°C, unless otherwise specified)

Symbol	Test Conditions	min.	typ.	max.	
I_S	V_{GS} = 0 V			32	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			128	A
V_{SD}	$I_F = I_S$, V_{GS} = 0 V, Note 1			1.5	V
t_{rr}	$I_F = I_S$, -di/dt = 100 A/ms, V_R = 100 V			250	ns
Q_{RM}			0.75		µC
I_{RM}			7.5		A

Note: 1. I_T test condition:
IXFR30N50: I_T = 15A
IXFR32N50: I_T = 16A

Note: 2. Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %

ISOPLUS 247 (IXFR) OUTLINE



1 Gate, 2 Drain (Collector)
3 Source (Emitter)
4 no connection

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	.244
R	4.32	4.83	.170	.190
S	13.21	13.72	.520	.540
T	15.75	16.26	.620	.640
U	1.65	3.03	.065	.080

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IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents:
4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

Figure 1. Output Characteristics at 25°C

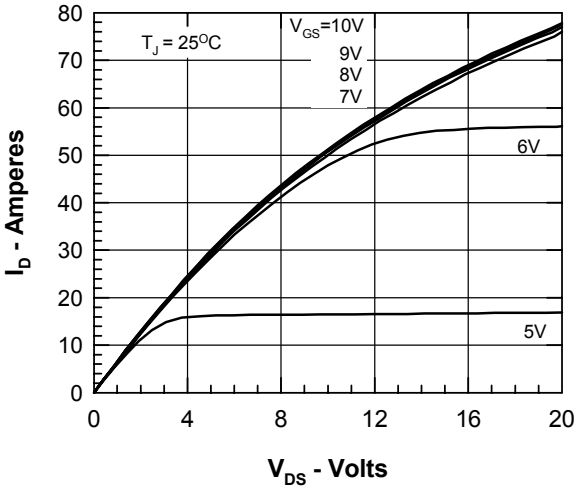

Figure 2. Output Characteristics at 125°C

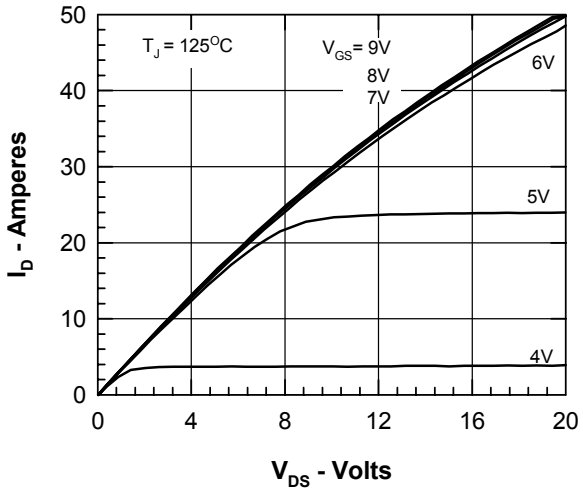

Figure 3. $R_{DS(on)}$ normalized to 15A/25°C vs. I_D

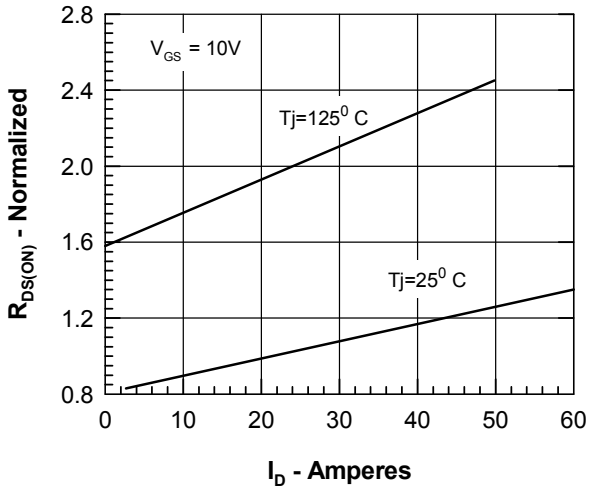

Figure 4. $R_{DS(on)}$ normalized to 15A/25°C vs. T_J

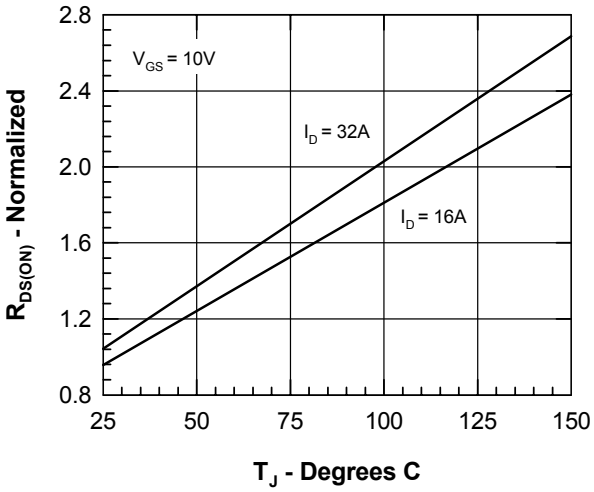

Figure 5. Drain Current vs. Case Temperature

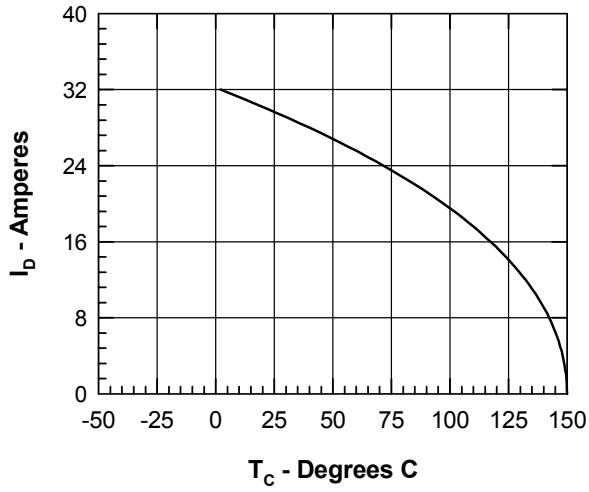

Figure 6. Admittance Curves

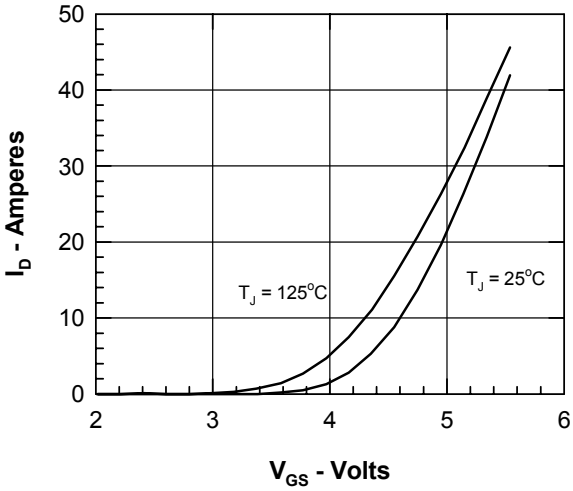

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Figure 7. Gate Charge

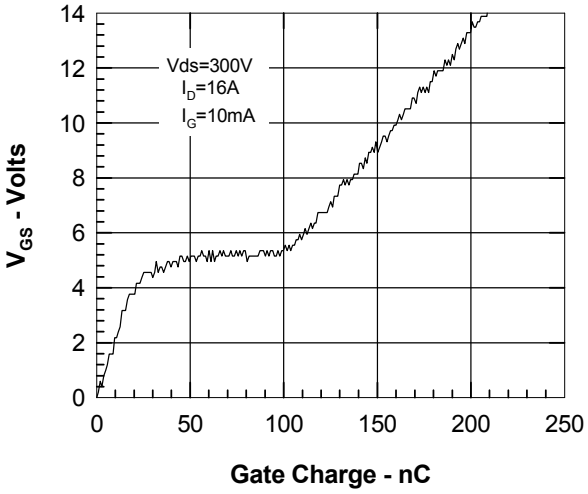


Figure 8. Capacitance Curves

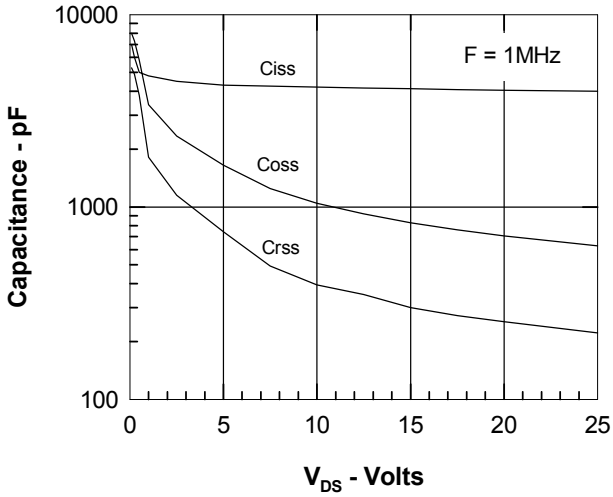


Figure 9. Forward Voltage Drop of the Intrinsic Diode

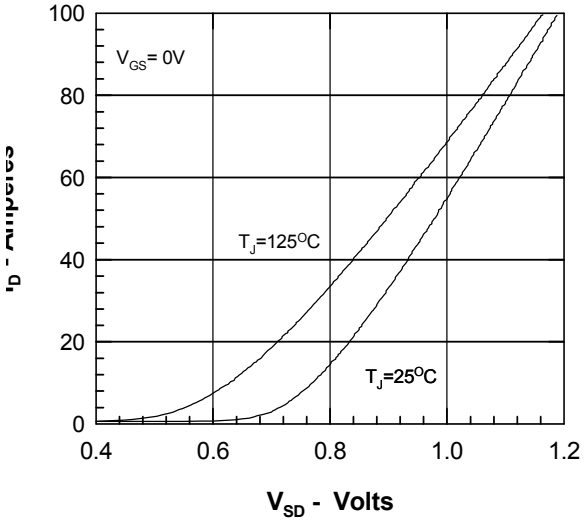
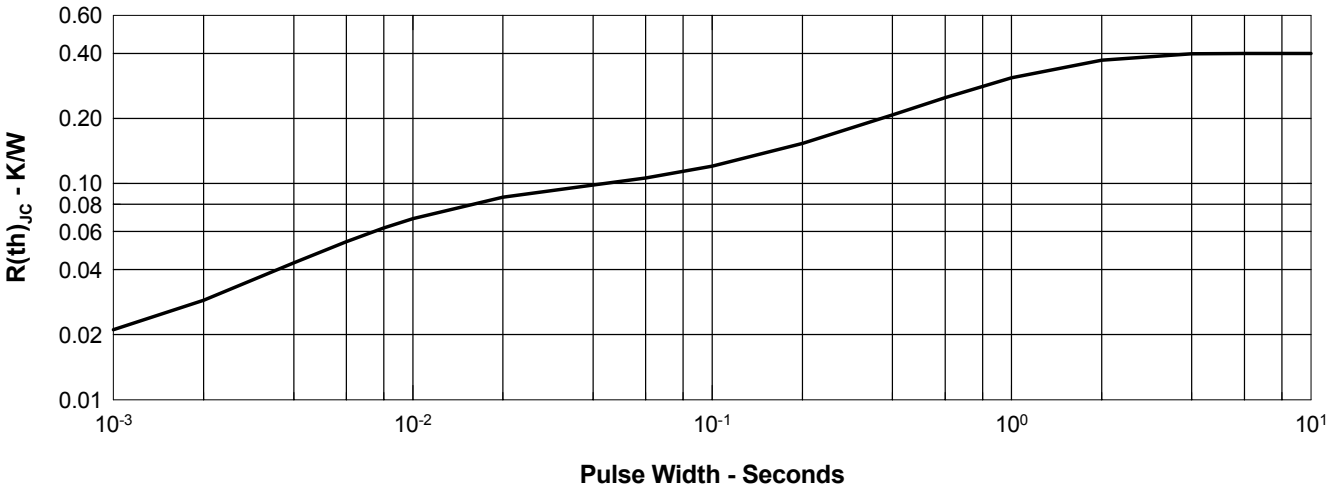


Figure 10. Transient Thermal Resistance



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